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| **FIM Conditioning board requirements** |

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# Introduction

The conditioning board or analog/digital filter wall aims to a potential free measurement, monitor and interlock signal splitting isolated from the original signals.

The signals identified to be connected to the conditioning board are defined where is needed a filtering, monitoring and isolated.

# Signal types

Typically the signals to be processed in the conditioning are identified as fast response and its requirements have been defined from the Fast Interlock Module signal list.

|  |  |
| --- | --- |
| Signal type | Description |
| Analogue input conditioning | |
| 0..10V | Solenoid current, Modulator I/V waveform |
| 1 Vpp | RF power detector, FMC ADC 3111 |
| 2 Vpp | RF Power detector FMC-116 |
| Digital isolation | |
| 24VDC to TTL/LVTTL | From PLC interface, CERN arc detectors |
| TTL/LVTTL to 24VDC | To PLC interface |
| TTL/LVTTL to TTL/LVTTL | Arc detector interfaces, LLRF |

Table 1 - Signal types

# Analog Input cond. board

The analogue conditioning board will be used to potential free measure, monitor and interlock analogue signals. Figure 1 shows a flow diagram of a single channel:



Figure - Analogue flow diagram

Analog type, characteristics and functions

|  |  |  |
| --- | --- | --- |
| Item | Value | Remarks |
| Power supply | 24 VDC  1 A, fused | Min 21.6V / Max 26.4V (+/-10%) |
| Connector | LEMO, 3-pin | Each channel has its isolated Ground |
| Input signal Bandwidth | 1 MHz | -3 dB Attenuation  The frequency cut of the amplifier is reduced by a high gain:  1MHz = G:1  100KHz = G:10  The gain factor and cut off frequency is constant and equivalent to 1MHz |
| Including the delay  Rise time | Less 1 us |  |
| Input Impedance | 1.0 MΩ | The impedance shall be reduced by setting an additional resistor on foreseen soldering socket. |
| Isolation Voltage | < 500V | Related to GND |
| Input Overvoltage Protection | YES |  |
| Power supply detection |  | Power supply status powered up |
| Output to FIM |  |  |
| Channel Gain | 1 (default) or  2, 5, 10 | Accuracy 1% |
| Output connector  Output connector | BNC  TBD | BNC, for local monitoring  TBD, for interfacing to FIM |
| Output signal level to FIM | TBD | The output signal will be conditioned to the ADC type, see section 5 |
| Output Signal Bandwidth to FIM | 1 MHz | -3 dB Attenuation  Single Pole Low Pass |
| Output noise level to FIM | < 0.1 % pp |  |

Table 2 - Analogue signal requirements

# Digital I/O cond. board

The Digital Front-End interface aims to isolate and protect the I/O module on the FMC – FPGA. The compatible interfaces were defined according to the I/O sensors listed on the signal list.



Figure – Digital front-end flow diagram

# FIM I/O and ADC Modules

There are two input types supported by the Fast Interlock Module (FIM), digital I/O and ADC. The conditioning board aims to support those modules according to the technical specifications below.

FMC116 – 16-channel, 14-bit ADC – 125 Msps:

<http://www.4dsp.com/pdf/FMC116_data_sheet.pdf>

* 62.5MHz bandwidth (DC)
* 2Vpp input range (1Vpp build option)
* (LV)TTL compatible trigger input, LVTTL trigger output.
* 0dBm clock input (typ.)
* +/- 1.25V offset correction (40uV steps)

ADC\_3111 – 8-channel, 16-bit ADC – 250 Msps:

<http://www.ioxos.ch/images/pdf/01_datasheet/ADC_3110_DS_A1.pdf>

* 1Vpp input range
* Single ended DC coupling
* External SSMC Clock reference

DIO (TBD)

Concerning the prototype design, there is also another ADC module which would be used on this stage.

NI 9223 – 4-channel, 16-bit ADC – 1 Msps:

<http://www.ni.com/datasheet/pdf/en/ds-260>

* +/- 10Vpp input range
* 60 VDC ch-ch isolation
* >1 Mhz bandwidth @ -3 dB
* Input impedance >1GΩ

# Design tool

We strongly recommended use Altium as standard design tool for PCB. According to the ESS Electronics Design Tool committee, Altium has been chosen as standard tool to exchange the projects, since this tool will be supported by ESS staff and its further maintainability or upgrades design.